Amendments to the Claims:

Claims 4-10 and 13-14 are pending, with claims 1-3 and 11-12 having been canceled, and claim 13 having been amended. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 - 3. (Canceled)

4. (Previously Presented) An array comprising:

a plurality of CMOS pixels, each CMOS pixel comprising:

a substantially square image sensing region, wherein a distance between the image sensing regions of neighboring pixels is optimized to reduce crosstalk between the neighboring pixels and the distance is at least 3.8 micrometers along a first axis and at least 4 micrometers along a second axis; and

a substantially hemispherical microlens positioned over the image sensing region of each pixel.

5. (Original) The array of pixels of claim 4, wherein the distance is further optimized to improve MTF.

6. (Previously Presented) An improved CMOS imaging array having a plurality of pixels for use in a CMOS imaging system, the improvement of each pixel comprising:

a substantially square image sensing region configured to increase the distance between the image sensing regions of neighboring pixels, wherein the distance is at least 3.8 micrometers along a first axis and at least 4 micrometers along a second axis; and

a substantially hemispherical microlens positioned over the image sensing region.

7. (Previously presented) The CMOS imaging array of claim 6, wherein the position of the substantially hemispherical microlens is configured to increase an effective fill factor.

8. (Previously presented) The CMOS imaging array of claim 7, wherein the improvement of each pixel further comprises:

a. a transfer transistor having a drain coupled to the cathode of the photodiode, a gate controlled by a control signal, Tx, and a source coupled to a floating sensing node;

b. a reset transistor having a drain coupled to a reset potential, a gate controlled by a control signal, Rx, and a source coupled to the floating sensing node; and

c. a source follower coupled between the floating sensing node and an output of the unit pixel, the source follower controlled by a select signal.

9. (Previously presented) The CMOS imaging array of claim 8, wherein the transfer transistor, the reset transistor, and the source follower are positioned along at least two sides of the pixel.

10. (Previously presented) The CMOS imaging array of claim 8, wherein the reset transistor is a depletion mode transistor.

11 - 12. (Cancelled)

13. (Currently Amended) The array of claim [[12]] 4, wherein the first axis and the second axis are perpendicular.

14. (Previously presented) The array of claim 4, wherein sides of each CMOS pixel are about 8 micrometers.